REMARKS

Applicants appreciate the Examiner's attention to the above referenced application. Reconsideration of the application is respectfully requested. Claims 1 and 3-32 were rejected. Claim 2 was cancelled. Claims 1 and 3-32 are now pending, of which claims 1, 14, 18 and 21 are independent.

35 USC § 103 Rejection of the Claims

Claims 1, 3-5, 7-10, 21-24, 26-29 and 32 were rejected under 35 USC § 103(a) as being unpatentable over Cypher (U.S. Publication No. 2004/0010610 A1), herein after referred to as Cypher, in view of Blake et al. (U.S. Publication No. 2004/0230751 A1) herein after referred to as Blake and Jennings III (U.S. Patent No. 6,134,631) herein after referred to as Jennings III. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Applicant's claim 1 includes, "logic, in response to receiving a write request referencing a block from a requesting processor core of the plurality of processor cores and the block not being owned, adapted to generate a first message including an invalidation part and a write-acknowledgement part, and wherein at least the invalidate part of the first message is to be delivered to ~~when received by~~ a second processor core of the plurality of processor cores ~~is~~ to invalidate the block in the second processor core and the at least the write-acknowledgement part of the first message is to only be delivered to[[, when received by]] the requesting processor core~~, is also~~ to act as a write acknowledgement to the requesting processor core." As can be seen, in applicant's claim 1 parts (an invalidation part and a write-acknowledgement part) of a

single message (the first message) is delivered to different processor cores (the second processor core and only the requesting processor core, respectively).

As the Office Action confirms at page 4, Cypher's invalidation message does not recite separate parts, but rather an invalidation message that is interpreted differently at a device to be invalidated versus D1 . Furthermore, applicants claim 1 includes the acknowledgement part of the first message is only delivered to the requesting core, as described in paragraph 0035-0036 of applicant's specification), while the same exact invalidate message is sent to both the requestor (D2) and the owner (D1) in Cypher. And Blake only describes combining snoop commands with snoop responses in a ring protocol, but doesn't disclose only delivering an acknowledgement part of a combined message to a requestor, while delivering an invalidate part of the message to another core, such as the second processor core in applicant's claim 1.

Applicant respectfully submits that applicant's claim 21 includes similar limitations to claim 1.

Claims 14 and 16-17 were rejected under 35 USC § 103(a) as being unpatentable over Blake et al. (U.S. Publication No. 2004/0230751 A1) herein after referred to as Blake in view of Jennings III (U.S. Patent No. 6,134,631) herein after referred to as Jennings III and Fletcher (U.S. Patent No. 4,445,174) herein after referred to as Fletcher. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Applicant's claim 14 describes a shared memory including receiving logic, ownership logic and eviction logic to "to generate an evict message referencing the address and the owning processor core in response to the receiving logic receiving the read request-and the ownership logic determining the owning processor core owns the block." The Office Action alleges Blake's

use of an IM Cast Out response is equivalent to such an eviction message. Yet, note that Black's IM Cast Out is merely a response from a receiving node that has the most recent cached copy of the address (i.e. response...when the IM bit is on, which indicates that this node was the most recent to cache new data and receiving new ownership {see paragraph 0055}). And as can be seen from paragraph 0055, only a single node may have the IM bit set. Therefore, Blake is only disclosing a scenario, where a receiving node provides a response (IM Cast Out) that it has the most recent cached copy for an address. In contrast, applicant's claim 14 is utilizing the shared memory (ownership logic) to determine an owning processor core and sending that owning processor core (referencing the owning processor core in) an eviction message.

As a specific illustrative example, assume that processor core R (requestor) is generating a request for address A and that processor core O (Owning) owns a cached copy of address A. Following the allegation used by the Office Action regarding Blake, processor core O receives the request and has the IM bit set, so it provides an IM cast out response to R to indicate it has the most recent copy. In contrast, according to an embodiment of applicant's claim 1, the request is received by a shared memory, the ownership logic included in the shared memory determines O's ownership, and the eviction logic in the shared memory generates an eviction message referencing O in response to the request and the ownership determination. As this example illustrates, the IM cast Out message from Blake is a response from an owner to the requestor to indicate it's IM bit is set, not an eviction message from a shared memory to (referencing) an owner, as in applicant's claim 1.

Claims 18-19 were rejected under 35 USC § 103(a) as being unpatentable over Blake et al. (U.S. Publication No. 2004/0230751 A1) herein after referred to as Blake in view of Bordaz et al. (U.S. Patent No. 6,195,728) herein after referred to as Bordaz and Jennings III (U.S. Patent No. 6,134,631) herein after referred to as Jennings III. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Applicant's claim 18 includes, " each of the plurality of blocks capable of being held in the shared memory by logic in the shared memory in: ... a present in the shared memory and owned by a core of the plurality of cores state." The Office Action alleges Blake's IM bit is equivalent to this state. However, the IM bit, as stated above, only indicates that the most recent copy is located in the node in question, but doesn't not indicate if it is also owned by a core, as in applicant's claim 18. In other words, assume the Office Action's allegation is taken from the perspective of applicant's shared memory being equivalent to a node SM (shared memory). Then, the IM bit being set in node SM (the shared memory) indicates the most recent copy for the address is in node SM (present). However, it doesn't indicate that the address is also owned by another node (a core in applicant's claim 18).

CONCLUSION

Applicant respectfully requests reconsideration in view of the remarks and amendments set forth above. If the Examiner has any questions, the Examiner is encouraged to contact the undersigned attorney at 503-712-4988. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0221 and please credit any excess fees to such account.

Respectfully submitted,

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